CLAIMS:

1. A processing apparatus conceived for processing data, based on control signals generated from a set of instructions being executed in parallel, comprising:

a plurality of issue slots, wherein each issue slot comprises a plurality of functional units, the plurality of issue slots being controlled by a set of control words, corresponding to the set of instructions,

characterized in that the processing apparatus further comprises a dedicated issue slot arranged for loading an immediate value in dependence upon a dedicated instruction comprising the immediate value.

2. An apparatus according to Claim 1, wherein the dedicated issue slot comprises a single functional unit arranged for only executing the dedicated instruction.

3. An apparatus according to Claim 1, further comprising a dedicated register file for storing said immediate value, the dedicated register file being accessible by the dedicated issue slot.

4. An apparatus according to Claim 1, wherein said processing apparatus is a VLIW processor and wherein said set of instructions is grouped in a VLIW instruction.

5. An apparatus according to Claim 4, wherein the VLIW instruction is a compressed VLIW instruction, comprising dedicated bits for encoding NOP operations.

6. An apparatus according to Claim 1, further comprising a register file associated with the plurality of issue slots.

7. An apparatus according to Claim 6, further comprising a connection network for coupling the plurality of issue slots and the register file.

8. A method for processing data, said method comprising the following steps:

- storing input data in a register file;
- processing data retrieved from the register file based on control signals generated from a set of instructions being executed in parallel, using a plurality of issue slots controlled by a set of control words being generated from the set of instructions;

and wherein each issue slot comprises a plurality of functional units,
characterized in that the method further comprises a step of loading an immediate value into a dedicated issue slot in dependence upon a dedicated instruction comprising the immediate value.

9. Instruction set, comprising a plurality of instructions for execution by a processing apparatus according to the preamble of Claim 1,
characterized in that the instruction set further comprises a dedicated instruction having an immediate value, which dedicated instruction when executed by a dedicated issue slot causes the dedicated issue slot to load the immediate value.

10. A computer program comprising computer program code means for instructing a computer system to perform the steps of the method according to Claim 8.

11. A compiler program product for generating a sequence of sets of instructions being arranged for execution by a processing apparatus according to the preamble of Claim 1, characterized in that the sequence of sets of instructions further comprises a dedicated instruction having an immediate value, which dedicated instruction when executed by a dedicated issue slot causes the dedicated issue slot to load the immediate value.

12. An information carrier comprising a sequence of sets of instructions being arranged for execution by a processing apparatus according to the preamble of Claim 1, characterized in that the sequence of sets of instructions further comprises a dedicated instruction having an immediate value, which dedicated instruction when executed by a dedicated issue slot causes the dedicated issue slot to load the immediate value.